Amendments to the Specification:

Page, 2, line 11, please amend the paragraph as follows

Figure 1 is a diagram illustrating an SRAM array comprising conventional single-port cells and split word lines. Each single-port cell 700 comprises six transistors that form a flip-flop circuit for storing data, which is formed by cross-coupling two logic inverters formed by transistors Q1D-Q4D, and two pass-gate transistors Q5D and Q6D. The source and drain of pass-gate transistor Q5D are connected between bit lines 720 and node ~~706~~706D. The source and drain of pass-gate transistor Q6D are connected between inverse bit lines 728 and node ~~710~~710D. Unlike a single word-line memory circuit, SRAM array 600 uses two word lines per row, word lines 724 and 730, each of which is connected to only one of the pass-gate transistors. Word line 724 is connected to the gate terminal of pass-gate transistor Q5D, and word line 730 is connected to the gate terminal of pass-gate transistor Q6D. In normal single port operation, data can be written to, or read from, each cell by asserting corresponding word and bit lines.

Page, 4, line 2, please amend the paragraph as follows:

The present invention provides a method and apparatus for reconfiguring a memory array. Aspects of the present invention include fabricating the memory array as at least one row of single-port cells up to a first metal layer. A split word line having first and second word lines is coupled to the single-port cells in each row, wherein the first word line is patterned in the first metal layer, and the second word line is patterned in a second metal layer. The split word line is further coupled to a spacer cell in the row. The method and apparatus further include programming the ~~base~~ memory array

into custom configurations based on whether the first and second word lines are connected over the spacer cell, or whether the first and second word lines are left unconnected.

Page 11, line 1, please amend the paragraph as follows:

Figure 5 is a diagram illustrating a basic layout of a row of cells after the single-port cells 400 are reconfigured as dual-port cells 408. Cell pairs X and Y are combined to form individual dual-port cells 408. Internal nodes within adjacent X and Y cell pairs are shown connected with internal node connections 404, preferably via 1 and metal 2. Word line A and word line B are shown unconnected over the spacer cell 406. Although not shown, bit lines, supply voltage VSS and VDD lines are also patterned in the array using via 1, metal 2, via 2 and metal 3. Bit lines are preferably metal 3 in this case.

Please amend the ABSTRACT as follows:

The present invention provides a method and apparatus for reconfiguring a memory array. Aspects of the present invention include fabricating the memory array as at least one row of single-port cells up to a first metal layer. A split word line having first and second word lines is coupled to the single-port cells in each row, wherein the first word line is patterned in the first metal layer, and the second word line is patterned in a second metal layer. The split word line is further coupled to a spacer cell in the row. The method and apparatus further include programming the ~~base~~ memory array into custom configurations based on whether the first and second word lines are connected over the spacer cell, or whether the first and second word lines are left

unconnected.